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Feature Article

Extreme temperature 6H-SiC JFET integrated circuit technology

Philip G. Neudeck[*,1], Steven L. Garverick[,2], David J. Spry[1], Liang-Yu Chen[3], Glenn M. Beheim[1], Michael J. Krasowski[1], and Mehran Mehregany[2]**

[1] NASA Glenn Research Center, 21000 Brookpark Road, M.S. 77-1, Cleveland, OH 44135, USA
[2] Dept. of Electrical Engineering and Computer Science, Case Western Reserve University, Cleveland, OH 44106, USA
[3] Ohio Aerospace Institute, NASA Glenn Research Center, 21000 Brookpark Road, M.S. 77-1, Cleveland, OH 44135, USA

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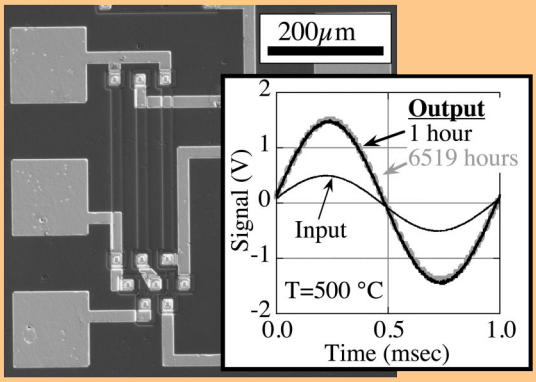
[*] Corresponding author: e-mail Neudeck@nasa.gov, Phone: +1 216 433 8902, Fax: +1 216 433 8643
[**] e-mail Steven.garverick@case.edu, Phone: +1 216 368 6436, Fax: +1 216 368 6888

Extreme temperature semiconductor integrated circuits (ICs) are being developed for use in the hot sections of aircraft engines and other harsh-environment applications well above the 300 °C effective limit of silicon-on-insulator IC technology. This paper reviews progress by the NASA Glenn Research Center and Case Western Reserve University (CWRU) in the development of extreme temperature (up to 500 °C) integrated circuit technology based on epitaxial 6H-SiC junction field effect transistors (JFETs). Simple analog amplifier and digital logic gate ICs fabricated and packaged by NASA have now demonstrated thousands of hours of continuous 500 °C operation in oxidizing air atmosphere with minimal changes in relevant electrical parameters. Design, modeling, and characterization of transistors and circuits at temperatures from 24 °C to 500 °C are also described. CWRU designs for improved extreme temperature SiC JFET differential amplifier circuits are demonstrated. Areas for further technology maturation, needed prior to beneficial system insertion, are discussed.



Optical micrograph of a 500 °C durable 6H-SiC JFET differential amplifier IC chip fabricated at NASA prior to packaging. Digitized waveforms measured during the 1st (solid black) and 6519th (dashed grey) hour of 500 °C operational testing show no change in output characteristics.

1 Introduction

1.1 High temperature IC applications The last three decades have witnessed a proliferation of performance-enhancing integrated circuit electronics into a wide variety of automotive, aerospace, deep-well drilling, and other industrial systems. This proliferation continues to accelerate, largely driven by the availability of increasingly capable lower-cost microelectronics coupled with the ever-growing demand for improved integrated system performance.

The presence of high temperatures, well beyond the limits of conventional electronics, is inherent to the operation of many important systems, particularly those involving fuel combustion (e.g., automotive and aerospace vehicles), high temperature manufacturing processes, and deep-well drilling [1–3]. When the temperature of the environment is too high, silicon-based microelectronic integrated circuits used to monitor and/or control crucial hot-section subsystems must reside in cooler areas that are either remotely located from the high temperature region or ac-

tively cooled with air or liquid cooling medium pumped in from elsewhere. However, these thermal management approaches introduce additional overhead that can negatively offset the desired benefits of the electronics relative to overall system operation. The additional overhead, in the form of longer wires, extra connectors, and/or cooling system plumbing, can add undesired size and weight to the system, as well as increased complexity, part count, and corresponding increased potential for failure. These difficulties stand as major hinderances towards expanded use of electronics to directly improve hot-environment system performance.

Despite these difficulties, the drive to put even more electronics into various applications, including subsystems that monitor and control high temperature areas of aircraft and automobiles, is unlikely to slow in the near future. A mere handful of high temperature electronics chips, perhaps purchased for a few hundred dollars, can enable millions of dollars of increased capability to a very large system. For example, directional and compositional telemetry made possible by ~200 °C high temperature electronics in a deep-well drilling operation can help prevent 10's to 100's of millions of dollars of loss in equipment and resources [4]. Similarly, improved weight, fuel economy, and maintenance over the multi-decade life of a commercial passenger aircraft would also translate into substantial operating cost savings. Even though high temperature ICs will never approach personal computer-chip volumes, these chips nevertheless can improve many products and systems that affect modern human life.

1.2 Extreme temperature IC technology Commercially available bulk silicon and silicon-on-insulator (SOI) metal oxide semiconductor field effect transistor (MOSFET) technologies are already satisfying important lower-power logic and signal processing requirements in the abovementioned industries up to 250 °C [1, 2, 5]. Extension of the IC operating temperature envelope to well above 300 °C would enable further improvements to some of these important systems. For example, telemetry systems for more aggressive and geothermal well drilling are likely to exceed 300 °C ambient temperatures, as will advanced jet-engine instrumentation and control. However, some fundamental material property limitations of silicon will likely preclude it from ever attaining prolonged IC functionality at temperatures well above 300 °C [1].

The emergence of wide bandgap semiconductors has facilitated semiconductor transistor and small IC demonstrations at extreme ambient temperatures of 500 °C or higher over the past two decades [6–17]. The vast majority of these reports have focused on current–voltage (I–V) properties and gain-frequency performance with little or no mention of how long such parts operated at high temperature. However, most envisioned applications require reliable operation over long time periods at high temperature, on the order of thousands of hours or more. Without such long-term durability, extreme temperature semiconductor ICs will not practically benefit (and will not be inserted into) the vast majority of important intended applications. Aside from work at the NASA Glenn Research Center [8, 16, 18–20], we are unaware of any published reports claiming stable semiconductor transistor operation for more than 10 hours at temperatures at or above 500 °C.

1.3 Technology selection – SiC JFETs In the nearer term, silicon carbide (SiC) appears to be the strongest candidate semiconductor for implementing highly durable/stable 300–500 °C integrated circuits. Competing wide bandgap semiconductors (such as III-N and diamond) are significantly less-developed, not available in bulk wafer form, and/or more susceptible to thermally driven chemical reactions and impurity diffusions that lead to unstable device performance over time while operating at extreme temperature.

While silicon electronics experience clearly demonstrates that complementary MOSFET (CMOS) technology is desired for implementing integrated circuits, development of the necessary high electrical quality gate-insulators that would enable long-term 500 °C operation of SiC MOSFETs will likely prove elusive for many years to come [21]. Similarly, the rectifying properties of SiC Schottky barrier gates are also susceptible to thermal degradation, which renders the metal–semiconductor field effect transistor (MESFET) a poor prospect for prolonged 500 °C integrated circuit transistors [19]. Transistor structures that operate solely using highly stable SiC pn junctions, like the bipolar junction transistor (BJT) and JFET, seem to offer the best chance for durable extreme temperature operation. Despite potential performance advantages, minority-carrier SiC BJTs [22] are more difficult to implement with predictable extreme temperature performance stability compared to majority-carrier SiC JFETs. For example, the BJT demands good ohmic contacts to both n-type and p-type SiC regions, whereas SiC JFETs can operate acceptably with quite non-ideal (even semi-rectifying) contact to its gate region. The development (by our group at NASA [23]) of very stable high temperature $Ti/TaSi_2/Pt$ ohmic contacts to n-type 4H-SiC and 6H-SiC is sufficient for n-channel SiC JFETs to be realized.

1.4 Article overview This article describes the state-of-the-art in extreme temperature (up to 500 °C) integrated circuits based on epitaxial SiC JFETs. It reviews recently published progress from the two research groups leading the development of this technology, namely the NASA Glenn Research Center and Case Western Reserve University (CWRU). Both groups have separately fabricated and tested similar discrete 6H-SiC JFET devices for low power signal conditioning. The NASA group packaged and tested transistors and very basic (i.e., few transistors) analog and digital integrated circuit chips for thousands of hours at 500 °C. The CWRU group has carried out extensive device and circuit modelling, particularly within the context of implementing high-gain differential amplifiers for use in

harsh-environment sensor signal conditioning. Experimental implementation of CWRU differential amplifier (diff-amp) circuits was verified using wafer-probed SiC JFET differential pairs (diff-pairs) residing on a hot chuck connected with external discrete circuit components.

2 Transistors

2.1 SiC JFET design and processing Driven by the primary need to realize integrated circuits with prolonged 500 °C operational durability, NASA initiated development of an epitaxial n-channel 6H-SiC JFET IC technology. Figure 1 schematically illustrates the basic cross-section of this JFET technology. The mesa-etched p^+ epi-gate structure avoids defects and extreme activation temperatures associated with high-dose p-type implants in SiC [24–27]. In contrast to p-type implants, nitrogen n-type source/drain contact implants activate at lower annealing temperatures (~1200 °C) with fewer defects [28, 29]. Despite inferior mobility compared to 4H-SiC, 6H-SiC was selected for initial work as having demonstrated slightly better structural stability during some thermal processing steps [30–33]. Implementation of this same JFET structure in the higher-mobility 4H-SiC will be attempted as part of future work. The backside metallization to the p-type substrate facilitates more direct control of the electrical potential of the p-type epilayer immediately beneath the JFET n-channel as well as direct electrical measurement of channel-to-substrate pn junction properties. The thickness and lighter doping of the p-type sub-channel layer keeps parasitic channel-to-substrate capacitance and FET body bias effect reasonably small. The Fig. 1 JFET structure also features a light-dose self-aligned nitrogen implant that reduces both parasitic resistance and electric field in the region between the gate finger and source/drain contact implants.

As shown in Fig. 1, a thermal SiO_2 layer passivates the top SiC surface of the JFET [34]. The highly durable metallization scheme of Ti/$TaSi_2$/Pt previously reported [23] contacted the n-type source/drain nitrogen implants and

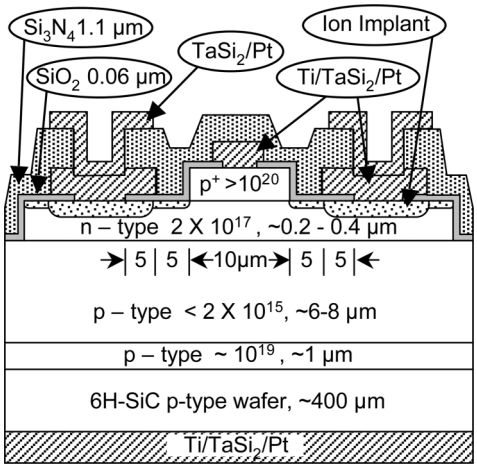


Figure 1 Simplified schematic cross-section of the NASA 6H-SiC JFET [34].

heavily p-type (Al-doped) gate epilayer. The Si_3N_4 layer was reactive sputter deposited at 200 W pulsed DC using a high-purity silicon target and injected N_2. Following patterned nitride via dry-etch, the wafer was annealed in an N_2 tube furnace for 30 minutes at 600 °C. Interconnects and wire bond pads were simultaneously formed by patterning $TaSi_2$/Pt on top of the Si_3N_4 dielectric. On-chip resistors were formed from the JFET n-channel layer and implants/contacts with the overlying p^+-gate layer removed. Further process details are described elsewhere [18, 20, 23, 34, 35].

The JFET fabrication process used in the CWRU work is based closely on that developed at NASA, as describe above, but was adapted for the micro-fabrication facility at CWRU. A 7.0 µm, Al-doped p^- epi SiC layer with a doping level of 2×10^{15} cm^{-3} was grown directly on the p-type SiC wafer. A 0.3 µm, n-epi SiC layer with a nominal doping density of 1×10^{17} cm^{-3} grown on the p^- bulk is used for the channel of the JFET, and a 0.2 µm p^+ epi SiC layer with a doping density of 2.0×10^{19} cm^{-3} grown on the n-channel is used for the gate of the JFET devices. The manufacturer of the SiC epi-wafers purchased by NASA and CWRU for this work specifies a ±50% variation in doping level and ±10% variation in thickness of the epilayers. Until more-uniform commercial SiC JFET epilayers become available, SiC integrated circuit designs will need to account for such variability of these important transistor parameters. No self-aligned implant was employed in the CWRU JFETs, and patterned aluminium was used for the source, drain, and gate contacts.

The channel doping concentration and thickness was chosen to assure negative values of threshold voltage for the n-channel depletion-mode JFET given wide variation of channel doping, thickness and operating temperature. The doping level of the gate layer is two or more orders of magnitude higher than the channel to ensure the depletion region formed by reverse bias gate voltage is primarily formed in the JFET channel. Also, a highly doped gate layer facilitates ohmic gate contacts. Since the p-type bulk sub-channel layer is lightly doped compared to the JFET channel, the depletion region due to reverse substrate bias is primarily formed in the bulk, thereby reducing the effect of the bulk on the device parameters. This lightly doped p^- epi SiC layer also results in lower bulk leakage currents.

2.2 High temperature packaging Long-term high temperature testing was limited to a few NASA chips that were bonded into custom high temperature ceramic packages. Probe-testing is not viable for carrying out accurate long-term electrical testing at 500 °C, as physical and electrical properties of probe tips rapidly degrade at these high temperatures leading to undesired probe-parasitic-dominated (instead of desired "device-under-test" dominated) measurements. Probe station testing was used for room temperature and short-term high temperature electrical measurements.

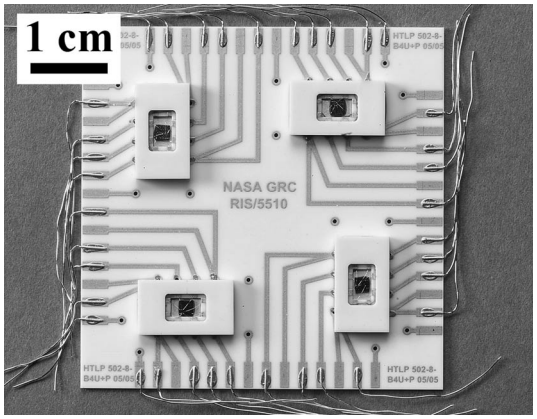


Figure 2 Four NASA SiC test chips as they were custom-packaged (without any lids, exposed to air during all testing) and mounted on a custom high-temperature circuit board. The ceramic chip-level packages and circuit board are based on 96% aluminum oxide and Au thick-film metallization.

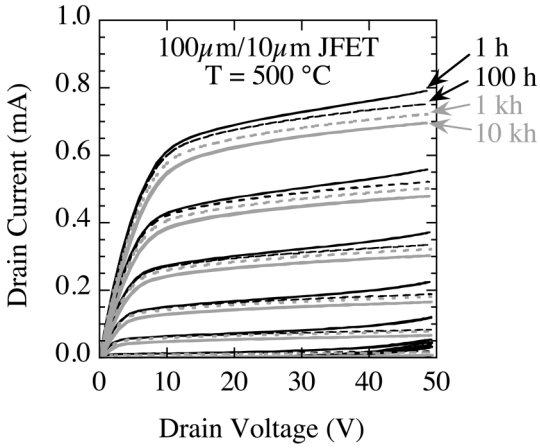


Figure 3 Drain I–V characteristics of packaged 100 μm/10 μm NASA 6H-SiC JFET measured during the 1st, 100th, 1,000th, and 10,000th hour of electrical operation at 500 °C. Gate voltage steps are –2 V starting from $V_G = 0$ as the topmost sweep of each curve.

The ceramic chip-level packages used for the NASA chips have been reported previously [8, 36–39]. The ceramic packaging material was 96% aluminum oxide (Al_2O_3) substrate and Au thick-film metallization. The SiC devices were electrically connected to each package's eight input/output terminals via 1 mil diameter Au wires. Chip packages were then attached to a ceramic printed circuit board also utilizing a 96% Al_2O_3 substrate and Au thick-film metallization. Figure 2 shows four SiC chips as they were custom-packaged (without any lids, exposed to air during all testing) and mounted onto the custom high-temperature circuit board. A few such boards were tested in laboratory box ovens. Au wires ~30 cm in length and 10 mil in diameter with glass fiber insulation sleeves were used to connect the circuit boards in the ovens to nearby terminal strips outside the ovens. The strips were then connected (via ~1 m length of RG-174/U coax cable or passive 10 MΩ oscilloscope probes) to computer-controlled test instruments. The SiC devices and circuits were operated continuously under electrical bias throughout the 500 °C test duration, with data measured and stored periodically (hourly at first, expanding to every 20 hours later). The atmosphere inside the oven was ordinary room air (approximately 21% O_2) without humidity control.

2.3 JFET 500 °C operational durability One of the NASA high temperature packaged chips shown in Fig. 2 contained two discrete 6H-SiC JFET's (one 200 μm/10 μm geometry shown in [34] and the other 100 μm/10 μm) that were extensively characterized and operated at 500 °C for 10,000 hours. These two JFETs featured contact pads large enough to support wire bonds directly on top of the active device mesa to facilitate long-term testing of intrinsic JFET behavior without possible interconnect-related parasitic leakage and capacitance. The 100 μm/10 μm packaged 6H-SiC JFET was operated and characterized via a 60 Hz linear-scale digitizing curve tracer operated with

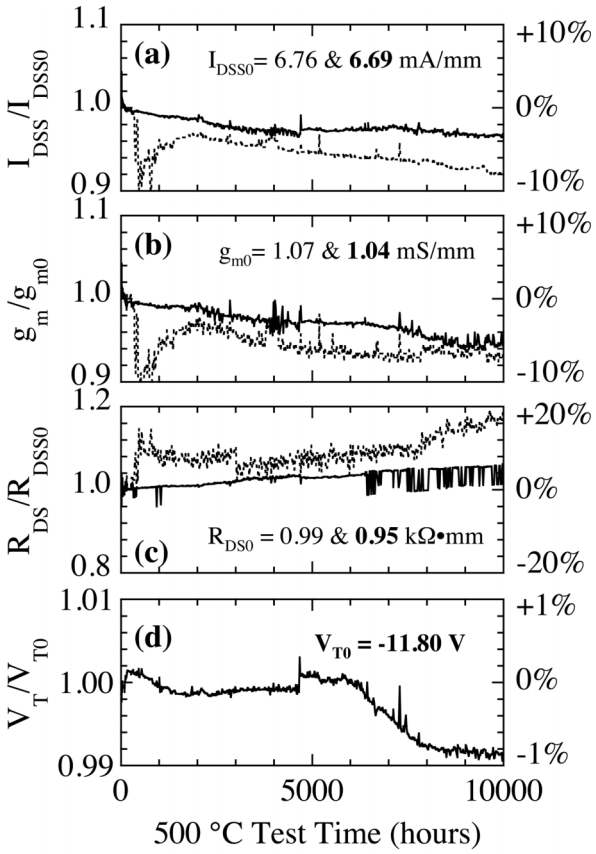


Figure 4 Normalized NASA JFET on-state parameters versus 500 °C test time through 10,000 hours for packaged devices with gate dimensions of 100 μm/10 μm (dashed, plain text, measured by curve-tracer) and 200 μm/10 μm (solid, bold text, SMU-measured). The plots are normalized to each transistor's measured value of I_{DSS0}, g_{m0}, R_{DS0}, and V_{T0} recorded at the 100 hour mark of 500 °C testing (i.e., after "burn-in").

50 V drain bias sweeps and –2 V gate steps from $V_G = 0$ V to $V_G = -16$ V. The 200 µm/10 µm packaged JFET was operated under $V_D = 50$ V and gate bias $V_G = -6$ V using computer-controlled DC source-measure units (SMUs).

As illustrated by the data presented in Figs. 3 and 4, the NASA discrete JFETs exhibited unprecedented high temperature operational stability and durability that exceeded 10,000 hours at 500 °C. Figure 3 compares drain current I_D versus drain voltage V_D characteristics of the 100 µm/10 µm JFET measured during the 1st, 100th, 1,000th, and 10,000th hours of 500 °C operation. Similar results were obtained for the SMU-measured 200 µm/10 µm JFET.

Figure 4 illustrates the measured variation of DC on-state I_{DSS}, transconductance g_m, drain-to-source resistance R_{DS}, and threshold voltage V_T for both packaged NASA Glenn JFETs as a function of 500 °C operating time through 10,000 hours. The Fig. 4 plots are normalized to each transistor's measured value of I_{DSS0}, g_{m0}, R_{DS0}, and V_{T0} recorded at the 100 hour mark of 500 °C testing (i.e., after "burn-in"). Figure 4a shows I_{DSS} recorded at $V_D = 20$ V, $V_G = 0$ V. Figure 4b shows the g_m benchmarked at $V_D = 20$ V from $V_G = 0$ V and –2 V steps, and Fig. 4c shows the time evolution of R_{DS}. The measured I_{DSS} and g_m changed by less than 10% over the course of the 10,000 hour 500 °C test. Figure 4d shows the precise time variation of V_T extracted from the computer-fit x-intercept of the SMU-measured $(I_D)^{0.5}$ vs. V_G of the 200 µm/10 µm JFET. The measured V_T changed by less than 1%. This excellent stability reflects the fact that JFET V_T is determined by the as-grown 6H-SiC epilayer structure.

2.4 SiC JFET models Compared to silicon, SiC has a wide bandgap voltage (~3 V as compared to 1.1 V) and has multiple donor levels which complicate the relationship between mobile carrier density and impurity concentration [13]. Despite this complication in carrier density, however, the current–voltage (I–V) characteristic of the SiC JFET can be well described using the conventional three-half (3/2) power model that was originally developed for long-channel silicon devices [40]. The model assumes a gradual channel, abrupt depletion layers, and constant mobility along the channel.

In the triode region (where $V_{DS} < V_{Dsat} = V_{GS} - (V_{bi} - V_{po})$) the drain current is given by

$$I_{DS} = \left(\frac{W}{L}\right) I'_P (1 + \lambda V_{DS}) \times \left[\frac{3V_{DS}}{V_{po}} - 2\left[\left\{\frac{(V_{DS} - V_{GS} + V_{bi})}{V_{po}}\right\}^{3/2} - \left\{\frac{(-V_{GS} + V_{bi})}{V_{po}}\right\}^{3/2}\right]\right] \quad (1)$$

where D, W and L are channel depth, width and length, respectively, V_{DS} is the drain-to-source voltage, V_{GS} is the gate-to-source voltage, V_{bi} is the built-in voltage of the gate/channel junction, V_{po} is the pinch-off voltage, I'_P is the normalized pinch-off current, and λ is the channel length modulation parameter of the JFET. The built-in voltage of the gate/channel junction, pinch-off voltage and pinch-off current are respectively given by

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right), \quad (2)$$

$$V_{po} = \left(\frac{qN_D D^2}{2\varepsilon_s}\right), \quad (3)$$

$$I'_P = \left(\frac{q^2 N_D n \mu_n D^3}{6\varepsilon_S}\right), \quad (4)$$

where N_A and N_D are the doping densities in the p^+-gate and n-channel, respectively. n_i is the intrinsic carrier concentration, n is the ionized carrier concentration in the channel, μ_n is the mobility of carriers (electrons) at a given temperature, k and q are Boltzmann and electron charge constants, and ε_s is the permittivity of 6H-SiC.

When $V_{DS} \geq V_{Dsat}$, the saturated drain current I_{DSAT} is

$$I_{DSAT} = \left(\frac{W}{L}\right) I'_P \times \left[1 - 3\left(\frac{-V_{GS} + V_{bi}}{V_{po}}\right) + 2\left(\frac{-V_{GS} + V_{bi}}{V_{po}}\right)^{3/2}\right](1 + \lambda V_{DS}). \quad (5)$$

Furthermore, when operating with small $(V_{GS} - V_T)$, typical of analog amplifiers, the square-law model accurately predicts the I–V characteristic of the JFET, which can be derived by Taylor series expansion near $V_{GS} = V_T$, yielding

$$I_{DSAT} = \frac{W}{L} k'(V_{GS} - V_T)^2, \quad (6)$$

where the threshold voltage is given by

$$V_T = V_{bi} - V_{po}, \quad (7)$$

and the transconductance parameter is

$$k' = \frac{3I'_P}{4V_{po}^2} = \frac{\mu_n \varepsilon_S n}{2DN_D}. \quad (8)$$

Experienced MOSFET designers will note the analogy to JFETs, where semiconductor permittivity replaces that of the gate dielectric, active layer thickness replaces dielectric thickness, and the addition of the ionization fraction (n/N_D). As in the MOSFET, the very important transconductance parameter g_m depends on device size and bias current as per

$$g_m = 2\sqrt{\frac{W}{L} k' I_{DS}}. \quad (9)$$

It is important to consider the effect of parasitic resistance in series with the JFET source and drains [41]. More specifically, parasitic source resistance R_S and drain resistance

R_D result from resistance of the SiC n-layers between edge of the gate to the edge of the source and drain contacts (a lateral channel distance of 5 µm + 5 µm in the Fig. 1 schematic) as well as non-zero contact resistance of the metal–semiconductor source and drain contact interfaces. These parasitic resistances degrade the JFET electrical characteristics by reducing the effective drain-to-source and gate-to-source voltages applied across the intrinsic JFET residing directly under the p^+-gate. (Note that R_D and R_S are only part of the total source-to-drain resistance R_{DS} of the device that also sums the resistance of the undepleted channel directly under the JFET gate.) Analogous parasitic resistances also exist in series with the gate and bulk of the device, but these have an insignificant effect on properly-biased device performance wherein gate-to-channel and channel-to-bulk reverse biased pn-junction leakage currents are small.

2.5 JFET temperature dependence Since n (number of ionized carriers), μ_n (mobility of electrons), and n_i (intrinsic carrier concentration) vary as a function of temperature T, the JFET device parameters that depend on these physical parameters have significant temperature dependence.

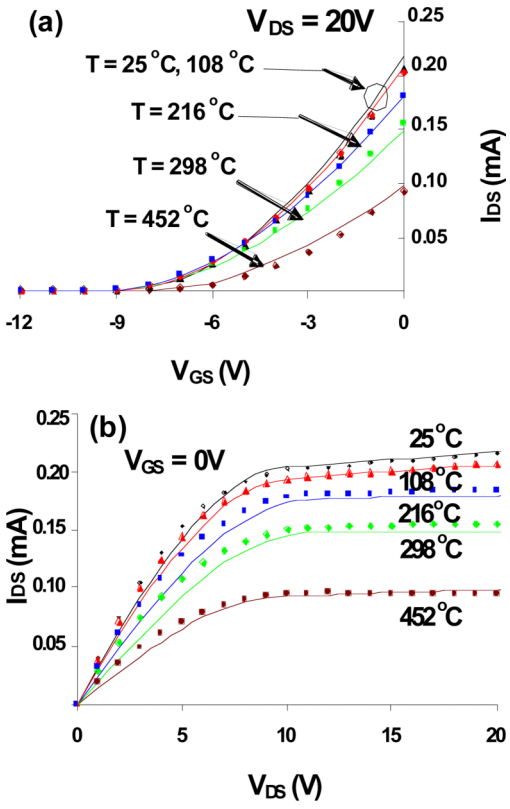


Figure 5 (online colour at: www.pss-a.com) Measured I–V characteristic of a typical CWRU fabricated 6H-SiC JFET with W/L = 100 µm/100 µm at various temperatures: (a) I_{DS} versus V_{GS} at V_{DS} = 20 V and (b) I_{DS} versus V_{DS} at V_{GS} = 0 V. Symbols mark measured values while solid curves show fit to the 3/2-power model [42].

Drain current (I_{DS}) versus gate-to-source voltage (V_{GS}) and drain-to-source voltage (V_{DS}) for a typical CWRU JFET measured at various temperatures are plotted in Fig. 5. The 6H-SiC JFET has well behaved I–V characteristics at temperatures up to 450 °C, although some instability was noticed at this highest temperature, almost certainly due to the instability of the Al metallization used in the CWRU prototypes. For each temperature T, the measured drain current was fit to the 3/2-power model and model parameters; V_{po}, I'_P, λ were extracted. During the fitting procedure, R_S and R_D were calculated based on the room-temperature measurements and theoretical temperature dependence of mobility. The measured JFET characteristic is well predicted by the 3/2-power model at all temperatures tested.

A summary of the extracted CWRU device parameters at various temperatures is presented in Table 1. The pinch-off current decreases with increases in temperature, i.e. I'_P at 450 °C is about half its value at room temperature, consistent with expected change in the $n\mu_n$ product. The change in pinch-off voltage is small as temperature increases from 25 °C to 450 °C. Variation in channel length modulation parameter (λ) with temperature is small and non-monotonic, potentially an artifact of the fitting procedure.

The threshold voltage V_T used in the square-law model (6) was computed using the extracted V_{po} values and compared to theoretical values using specified epitaxial thickness and impurity concentration. The measured V_T falls within the range that is calculated from (2), (3) and (7) given manufacturing tolerances, for all temperatures up to 450 °C, with a temperature dependence of –2.3 mV/°C exhibited up to 300 °C.

Figure 6 quantifies the measured temperature dependence of R_{DS}, g_m (at V_D = 20 V from V_G = 0 V and V_G = –2 V step data), and I_{DSS} (I_D at V_D = 20 V, V_G = 0 V) for the two packaged NASA JFETs. The parameters in Fig. 6 are normalized to a transistor gate width of 1 mm. I_{DSS} and g_m exhibit a nearly 3.5-fold decrease as temperature is increased from 25 °C to 500 °C, while R_{DS} increases by approximately the same factor. Such closely coupled behavior reflects the fact that these parameters are dominated by the same n-channel properties of decreasing mobility with increasing ionized carrier concentration as temperature is increased [13–15]. The threshold voltage V_T of the NASA devices (not plotted) becomes more negative linearly at a

Table 1 Extracted device parameters for a typical CWRU-fabricated 6H-SiC JFET with W/L = 100 µm/100 µm at various temperatures [42].

temperature (°C)	I'_p (mA)	V_{po} (V)	λ (V^{-1})	$R_{S,D}$ (kΩ)
25	0.48	11.90	0.0064	4.54
108	0.45	12.00	0.0068	4.64
216	0.44	12.40	0.0031	6.63
298	0.39	12.50	0.0008	8.90
452	0.26	11.13	0.0066	13.39

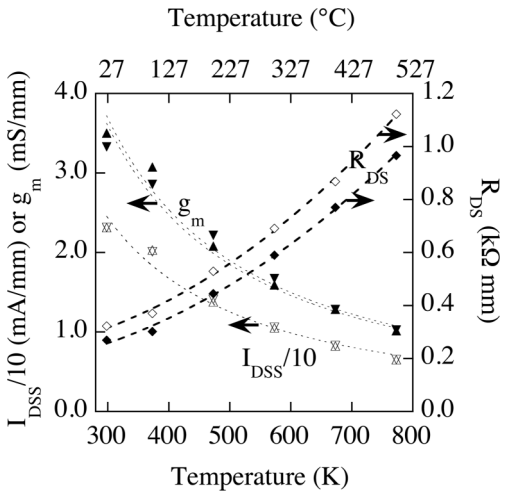


Figure 6 Temperature dependence of measured on-state parameters (normalized to 1 mm gate width) of I_{DSS} (open triangles), g_m (filled triangles), and R_{DS} (diamonds) for both packaged 6H-SiC JFETs made by NASA. For I_{DSS} and g_m, fits proportional to $T^{-1.3}$ (in Kelvin) are shown by the dashed lines, whereas the dashed-line fits shown for R_{DS} are second order temperature polynomials (also in Kelvin) [20].

slope of −1.6 mV/°C as temperature increases from 24 °C to 500 °C.

The dashed lines shown in Fig. 6 illustrate first-order approximation fits to the NASA experimental data that can be rapidly incorporated into SPICE circuit simulation code [43–45]. For I_{DSS} and g_m, fits proportional to $T^{-1.3}$ (in Kelvin) are shown, whereas the fits shown for R_{DS} are second order temperature polynomials (also in Kelvin). R_{DS} and *n*-channel resistors can be approximated by the SPICE semiconductor resistor model with SPICE parameters R_{SH} (sheet resistance) = 8 kΩ/square, TC1 = 2.5 K^{-1} and TC2 = 5.3×10^{-6} K^{-2}. The basic SPICE JFET model does not include FET substrate bias body effect and temperature-dependent channel conduction.

Since the NMOS LEVEL 1 SPICE transistor model does include non-negligible body bias and temperature-dependent channel conduction effects, the NMOS model provides more accurate first-order SPICE modeling of NASA transistors provided that JFET gates are operated in reverse bias with low leakage relative to n-channel conduction current. This is because the drain current of both JFETs and MOSFETs (long channel, operating in the saturation on region) is approximated by [44]:

$$I_D = \frac{I_{DSS}}{V_T^2}(V_G - V_T)^2(1 + \lambda V_D)\,. \tag{10}$$

For the NASA-fabricated 6H-SiC JFET devices the measured λ (SPICE LAMBDA) was ~0.005 V^{-1}, while the measured FET body effect coefficient (SPICE GAMMA) was ~0.3 $V^{-1/2}$. These two parameters exhibited negligible change between 25 °C and 500 °C.

Prior studies comparing 6H- and 4H-SiC JFET performance indicate that somewhat different SPICE parameters and temperature behavior will apply when 4H-SiC JFETs are experimentally implemented [46]. Indeed, somewhat different quantitative changes in measured parameters as a function of temperature become evident even when comparatively scrutinizing the similarly-fabricated NASA and CWRU 6H-SiC JFET results summarized in this section. For example, the I_D at V_D = 20 V and V_G = 0 V (i.e., I_{DSS}) drops ~30% between room temperature and 298 °C for the CWRU 6H-SiC JFET (Fig. 5), whereas the NASA 6H-SiC JFET exhibited a ~50% drop over nearly the same temperature range (I_{DSS} of Fig. 6). Thus, further work is needed to quantitatively understand the relative contributions of various experimental differences, especially with respect to the JFET processing differences mentioned in Section 2.1. Nevertheless, all JFET devices in this work (as well as previous SiC JFET work [6, 10, 13–15, 46–48]) exhibit qualitatively similar trends of significantly decreased drain current and gain (with increased parasitic resistances) as temperature increases, primarily due to decreasing conductivity of the n-channel layers in the devices.

3 Circuits

3.1 Amplifiers High-temperature, smart sensors are needed in propulsion and power instrumentation applications, for example, to enable optimized fuel efficiency, reduced emissions, and improved safety. The ability to use electronic sensing systems at elevated temperatures would not only make new products possible, but would also decrease costs of current products by eliminating large, heavy, complex cooling systems. Reliability would be improved by reducing the weight of cabling and the number of interconnections to remote electronics, and there would be less noise and interference in the signals acquired using interface electronics that are placed in close proximity to the sensor.

Ground noise and parasitic capacitance can be reduced by careful placement and routing of components, specifically by placing the sensor in close proximity to the amplifier to reduce parasitic capacitance and minimize reception of man-made interference. It is important to use a differential frontend with high-impedance input devices to minimize the flow of current on the ground line, which serves as a signal reference. In a high-temperature sensing application, the differential frontend should operate in the high-temperature environment of the sensor, but the backend of the amplifier may operate in a room-temperature environment, with minimal effect on input-referred noise.

The schematic and SEM micrograph of a SiC JFET differential pair fabricated at CWRU having W/L = 110 μm/10 μm and series resistance is presented in Fig. 7. The gain of a single-stage amplifier is limited by the $g_m r_0$ product of its input pair, and unity-gain bandwidth of the amplifier is generally given by g_m/C where $g_m = G_m$ is the transconductance of the differential pair, r_0 is the transistor

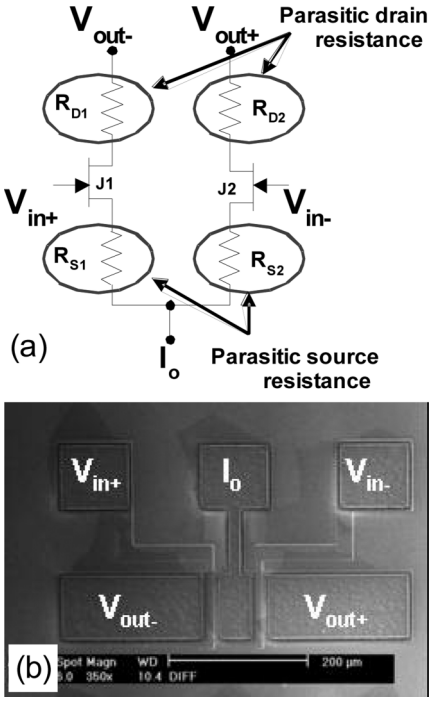


Figure 7 SiC differential pair fabricated at CWRU with W/L = 110 µm/10 µm: (a) Schematic, and (b) SEM micrograph. Modified from [49].

output resistance, and C is the compensation/load capacitance, depending on the amplifier topology used. The offset voltage of the differential pair contributes directly to the input-referenced offset voltage of the amplifier.

In this section, the electrical characterization of a CWRU-fabricated 6H-SiC JFET differential pair carried out using a probe station with hot chuck for temperatures up to 450 °C is presented. The DC transfer characteristic of the differential pair is measured to evaluate its transconductance (G_m) and offset voltage (V_{os}). In order to ensure that transistors operate in the saturation region, V_{DG} must be greater than $-V_T$. More specifically, the differential pair was operated in these tests with the inputs $V_{in+/-}$ biased at ground, outputs $V_{out+/-}$ biased at 30 V, and bias current I_0 was stepped from 10 µA to 500 µA.

The DC transfer characteristic of a typical CWRU-fabricated differential pair at room temperature and 450 °C is illustrated in Fig 8. A comparison of Fig. 8a and b reveals that the offset voltage of the differential pair increases with bias current, which is thought to be dominated by the mismatch in the parasitic source resistance $R_{S1,2}$ in this prototype wafer. A comparison of Fig. 8a and c reveals the expected decrease in transconductance (slope) with increasing temperature, although the maximum differential current is determined by the ideal current source used in this experiment. Also, given comparable bias currents, it is observed that the input offset voltage at 450 °C is higher than that at room temperature. This is expected, since sheet resistance increases with temperature, which leads to increased mismatch between $R_{S1,2}$. Despite the high resistance of the n-channel layer, the offset voltage of the differential pair could be greatly reduced given more accurate mask alignment, or by using structures that are relatively insensitive to alignment errors. A self-aligned n-type implant following patterning of the p^+-gate would also reduce R_S and offset voltage.

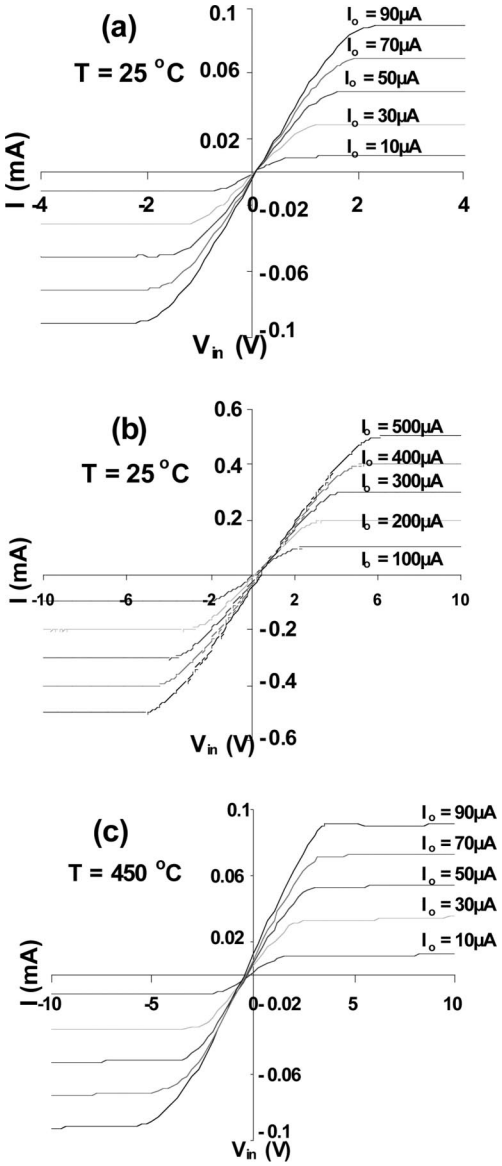


Figure 8 Measured DC transfer characteristics of a typical CWRU 6H-SiC JFET differential pair with W/L = 110 µm/10 µm for various bias currents at (a) and (b) room temperature, and (c) at 450 °C [50].

The transconductance of the differential pair is calculated from the slope of the DC transfer characteristic and is presented in Fig. 9 using data from the same differential pair at room temperature and at 450 °C, for various bias currents. At 450 °C, G_m is about half its value at room temperature, as expected from the temperature trend of the $n\mu_n$ product. The shift in the offset voltage at higher bias currents and at 450 °C is also apparent.

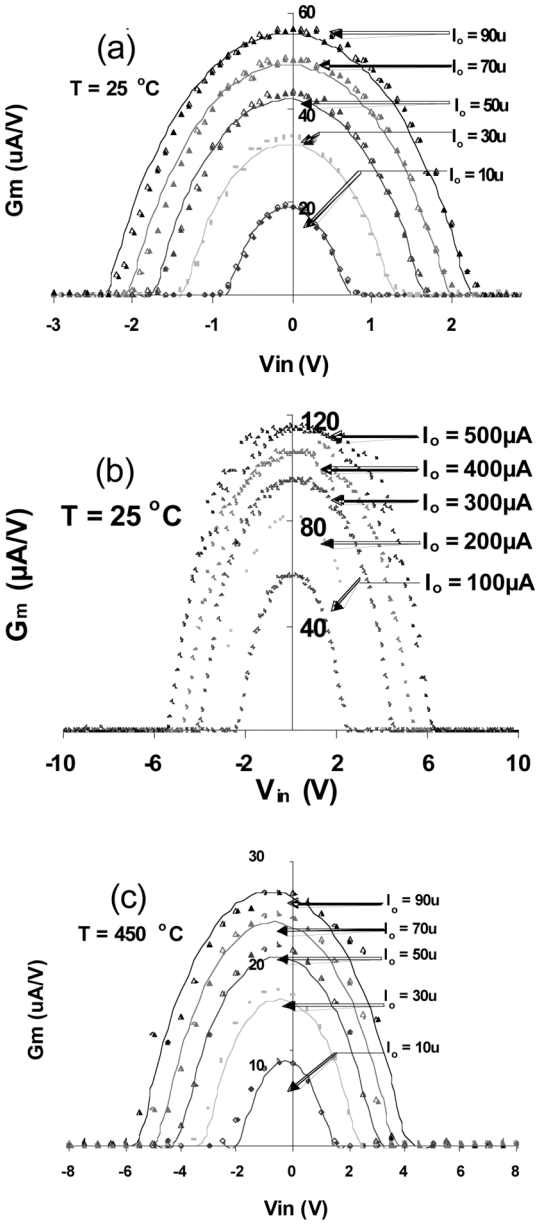


Figure 9 Measured transconductance (G_m) of the CWRU 6H-SiC differential pair with W/L = 110 μm/10 μm for various bias currents at (a) and (b) room temperature, and (c) at 450 °C [50].

3.1.1 Multi-stage differential amplifier using external biasing and passive loads The circuit schematic of a three-stage differential amplifier using SiC differential pairs with external bias currents and passive load resistors is shown in Fig. 10. The low-frequency (LF) voltage gain of the differential amplifier is given by

$$A_0 = \prod_{i=1}^{n} (G_{mi}(R_{Li} \| r_{0i})) , \tag{11}$$

where G_{mi} is the transconductance and r_{0i} is the small-signal resistance of the SiC differential pair, and R_{Li} is the load resistance, in the i-th stage. The amplifier gain-

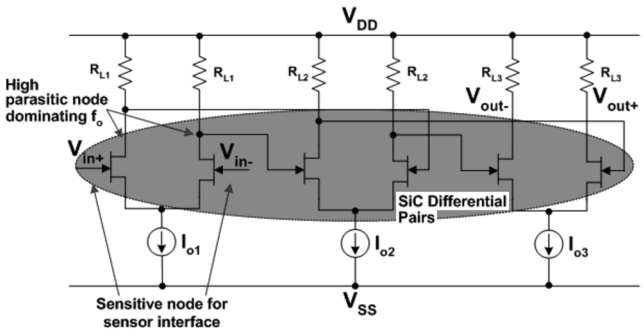


Figure 10 Schematic of three-stage differential amplifier using CWRU-fabricated 6H-SiC JFET differential pairs connected via probe station with external bias supplies and load resistors [49].

bandwidth in this configuration is limited by the parasitic capacitance (C_L) in the interconnection to the off-chip passives and is given by

$$\omega_0 \approx (G_{mi}/C_{Li}) . \tag{12}$$

The amplifier input offset voltage is dominated by the offset voltage of the first stage. To obtain low input-offset voltage and minimize supply voltage requirement, bias current in this stage should be small. However, bias current also determines G_m of the differential pair, and should be high to achieve high amplifier bandwidth.

In these tests, the bias currents were chosen for high gain and bandwidth at elevated temperatures, while allowing DC coupling between stages, by setting the drain of each JFET to a potential greater than $-V_T$ above its gate potential. A single-stage differential amplifier uses I_0 = 100 μA, R_L = 470 kΩ, V_{SS} = 0 V, and V_{DD} = 50 V. A two-stage amplifier uses I_{01} = 200 μA, I_{02} = 100 μA, R_{Lx} = 470 kΩ, V_{SS} = 0 V, and V_{DD} = 75 V, and a three-stage configuration was constructed using I_{01} = 300 μA, I_{02} = 200 μA, I_{03} = 100 μA, R_{Lx} = 470 kΩ, V_{SS} = 0 V, and V_{DD} = 100 V (Fig. 10). As such, for all stages of all amplifiers, there is approximately a 25 V bias from drain-to-gate of each differential pair. This far exceeds the required voltage ($V_{DG} > -V_T$) for saturated operation so supply voltage could be reduced if desired, but the devices tested did not fail at this high supply voltage, even at elevated temperatures.

The frequency response of one, two and three-stage cascades at room temperature and at 450 °C was tested using the setup illustrated in Fig. 11. Feedback resistors R_f and R_{in} provide biasing that cancels the input-referred differential offset voltage of the amplifier, and also provide the common-mode level shifting necessary to bring the high common-mode level of the output down to a low level at the input that insures that all transistors operate in saturation. Capacitor C_{in} is used to couple a low-magnitude, ac test signal to the input of the amplifier under test. Given very large values of input coupling capacitor and feedback bias resistors, the open-loop response of the amplifier is obtained by examining the amplifier output.

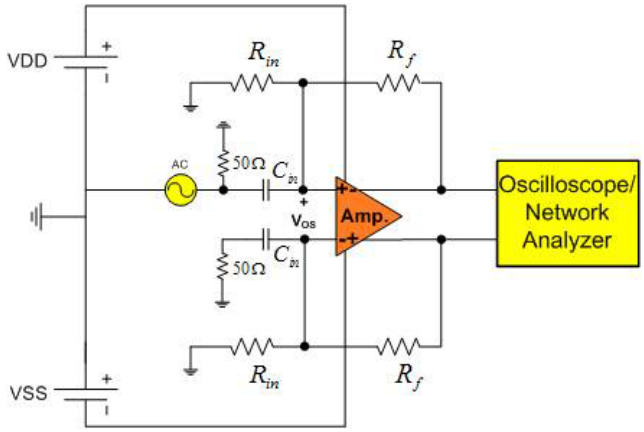


Figure 11 (online colour at: www.pss-a.com) Test setup used for the one-, two-, and three-stage differential amplifiers.

The measured frequency response is presented in Fig. 12. For the three-stage amplifier at room temperature, the reduced voltage gain at low-frequency is caused by the feedback biasing technique used to stabilize the operating point. The low-frequency gain and unity-gain frequency for the three-stage amplifier are approximately 50 dB and 200 kHz, respectively, at 450 °C.

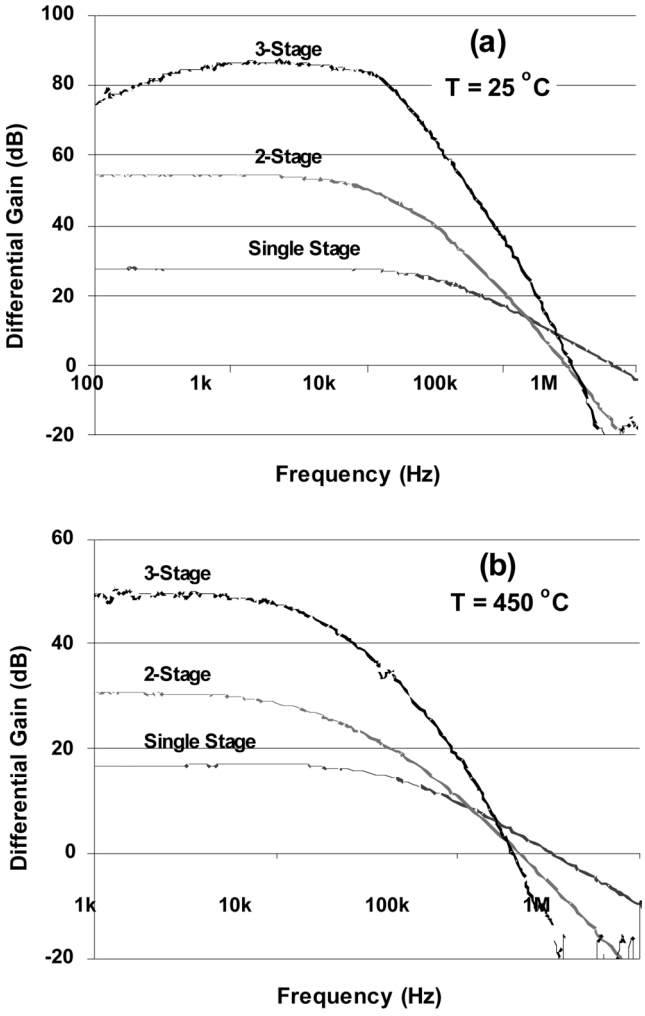


Figure 12 Measured frequency response of a CWRU multi-stage differential amplifier circuit (a) at 25 °C and (b) at 450 °C [49].

3.1.2 Multi-stage differential amplifier using external biasing and active loads The low-frequency voltage gain of the differential amplifiers discussed in the preceding section is limited by the $g_m r_0$ product of the SiC differential pair, which is given by

$$g_m r_0 = 2\sqrt{\frac{W}{L}k' I_{DS}}\,\frac{1}{\lambda I_{DS}} \propto \sqrt{\frac{1}{I_{DS}}}\ . \tag{13}$$

Thus, for a given device size, the bias current of the differential pair must be reduced in order to achieve high voltage gain. This results in smaller input offset voltage, at the cost of reduced g_m, and lower amplifier bandwidth. In order to achieve both high voltage gain and bandwidth, a different topology which is relatively insensitive to the poor r_o of the SiC JFET is needed. One such topology is illustrated in Fig. 13.

In this circuit, the output of the SiC differential pair is connected to the input of an external (commercial) opamp, which is configured as a transresistance stage that holds the JFET drain at a virtual ground. For $Z_f = R_f \,||\, (1/sC_f)$,

$$\left|\frac{V_{out}(s)}{V_{in}(s)}\right| = \frac{g_m\left[\dfrac{R_f}{1+sR_fC_f}\right]}{1+\dfrac{s}{\omega_0}\left[1+sC_P\left(\dfrac{R_f}{1+sR_fC_f}\right)\right]}$$

$$= \frac{g_m R_f}{\dfrac{s}{\omega_0}R_f(C_f+C_P)+s\left(\dfrac{1}{\omega_0}+R_fC_f\right)+1}\ , \tag{16}$$

where s is the complex signal frequency, ω_0 is the unity-gain frequency of the external opamp, which is assumed to be internally compensated using single-pole roll-off. Equating this to the canonical form with low-frequency gain A_0 and quality factor Q,

$$\left|\frac{V_{out}(s)}{V_{in}(s)}\right| = \frac{A_0}{\dfrac{s^2}{\omega_n^2}+\dfrac{s}{Q\omega_n}+1}\ , \tag{17}$$

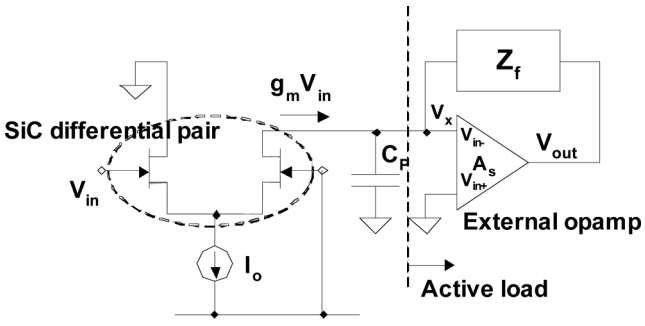


Figure 13 SiC amplifier topology with active load [42].

yields

$$\omega_n = \sqrt{\frac{\omega_0}{R_f (C_f + C_P)}} \approx \sqrt{\frac{\omega_0}{R_f C_P}} \tag{18}$$

for $C_f \ll C_P$, and

$$Q = \frac{1}{\frac{1}{\omega_0} + R_f C_f} \frac{1}{\omega_n} \approx \frac{\sqrt{\omega_0 R_f C_P}}{1 + \omega_0 R_f C_f} . \tag{19}$$

In other words, the 3 dB bandwidth can be extended to the geometric mean of the natural frequency of the passive elements ($1/R_f C_p$) and the unity-gain frequency of the external opamp, while Q can be set to 1 for critical damping, through proper choice of C_f.

A two-stage hybrid differential amplifier based on this topology is presented in Fig. 14. In this approach, only the two SiC differential pairs would reside in the hot zone with the harsh-environment sensor, while the rest of the circuit (active loads) reside in a cooler conventional electronics environment. The low-frequency voltage gain of each stage is given by $G_m R_f$, where G_m is the transconductance of the SiC differential pair, and R_f is the external feedback resistor. The bias current I_0, and feedback resistor are chosen such that voltage gain of 100 can be obtained from a single stage. Low bias currents are favorable from the perspective of small input-referred offset, and power supply needed to keep devices saturated. Load resistor R_L is chosen to enable DC coupling between stages while maintaining devices in saturation region. More specifically, a V_{DG} of 12.5V was chosen in order to maintain low supply voltages.

It was observed that the G_m of the differential pair is ~40 μS for a bias current of 50 μA at room temperature, and ~21 μS at 450 °C. Therefore, for this bias current, $R_f = 2.5$ MΩ is needed to achieve the desired low-frequency voltage gain of 100 at room temperature. The expected single-stage voltage gain at 450 °C is ~53. A two-stage configuration with identical stages would yield a voltage gain of ~80 dB at room temperature, and ~69 dB at 450 °C.

The theoretical unity-gain frequency is the geometric mean of the differential pair bandwidth (g_m/C_P) and bandwidth of the external opamp (ω_0), where C_P is the parasitic capacitance at the drain of the SiC differential pairs. At 450 °C, the bandwidth would degrade ~$\sqrt{2}$, due to the g_m reducing to half its value at room temperature. A 0.5 pF feedback capacitor C_f was used to reduce peaking in the amplifier frequency response. The external opamp used in this design, the TE 2072, has a unity-gain bandwidth of 10 MHz. In summary, for the design illustrated in Fig. 14; $V_{DD} = 15$ V, $V_{SS} = -15$ V, $V_+ = 5$ V, $R_L = 330$ kΩ, $R_f = 2.5$ MΩ, and $C_f = 0.5$ pF.

The measured frequency response of the Fig. 14 amplifier circuit at SiC diff-pair temperatures of 25 °C and 450 °C is presented in Fig. 15. At room temperature, the measured LF voltage gain from the single-stage amplifier is 40 dB, and from a two-stage amplifier is ~80 dB, as expected. The reduced gain at low frequency from the two-stage is due to the feedback biasing technique used to conduct the tests (not shown), which adds a dominant pole at ~16 Hz given a 1 MΩ feedback resistor and input coupling capacitance of 100 μF. The measured bandwidth of the differential amplifier at room temperature is ~1.8 MHz, so the expected bandwidth at 450 °C is ~1.3 MHz; consistent with measurement. The gain-bandwidth product is about ~1300 kHz, which at this writing is a state of the art metric for a circuit with $T > 300$ °C SiC differential pair sensor input.

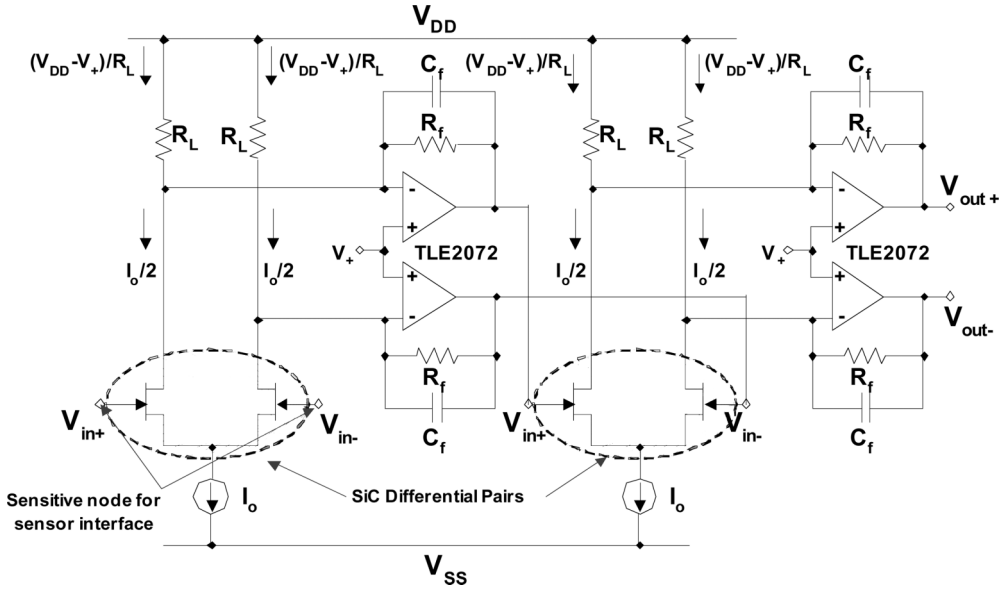


Figure 14 Schematic of the hybrid two-stage differential amplifier with active loads. The circled SiC differential pairs operate at high temperature, while the rest of the circuit resides in a cooler conventional electronics environment [42].

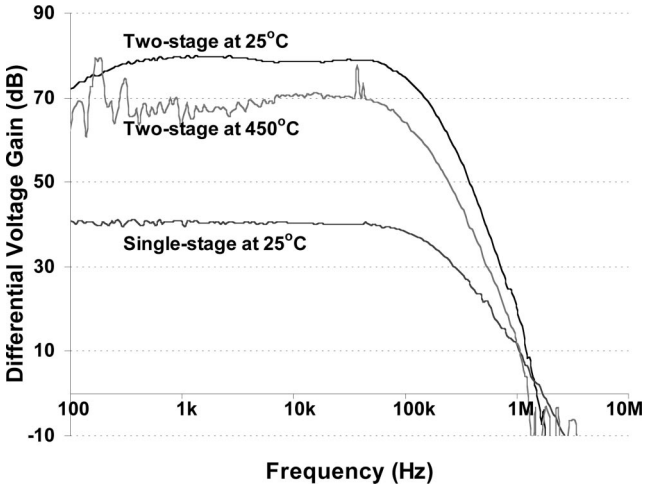


Figure 15 Measured AC response of the active load hybrid differential amplifier (Fig. 14) with SiC differential input pairs at room temperature and at 450 °C [42].

3.1.3 Single-chip SiC amplifiers Single-chip prototype amplifier stage integrated circuits were fabricated, packaged, and electrically tested for thousands of hours in a 500 °C oven at the NASA Glenn Research Center. On-chip resistors were formed from the JFET n-channel layer and implants/contacts with the overlying p^+-gate layer removed. The NASA prototype integrated circuits were only intended to demonstrate prolonged operational durability at 500 °C, and thus were not optimized for signal gain or frequency performance.

Figure 16 shows gain vs. frequency characteristics measured at 25 °C and 500 °C from a packaged inverting amplifier (inv-amp) IC formed from an 80 µm/10 µm JFET (with two 40 µm/10 µm gate fingers) interconnected to a 20-square n-channel SiC load resistor on the same chip. A 1 V peak-to-peak sine wave test input was applied with −5 V DC bias and the V_{DD} supply voltage was 40 V with chip substrate grounded. Relatively large and temperature-

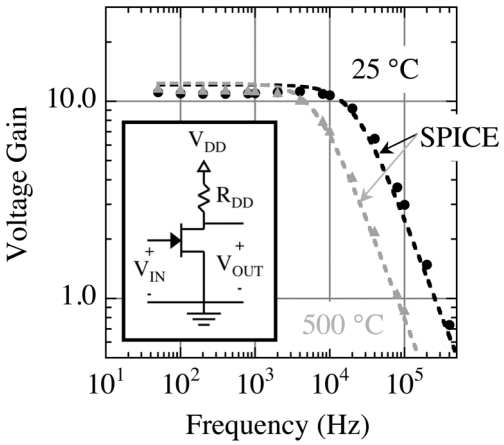


Figure 16 Measured (points) and SPICE-modeled (dashed lines) gain-frequency characteristics of NASA prototype 6H-SiC inverting amplifier IC at 25 °C (black) and 500 °C (grey) [20].

independent stray capacitances are expected to arise from the oven test setup that features many long (~30 cm) unshielded Au wires running in and out of the test oven in close-proximity to each other. Using a 100 kHz capacitance meter, the effective capacitance at this particular inverting amplifier's output terminal was measured to be 55 pF with the 11 pF, 10 MΩ oscilloscope signal measurement probe connected.

Figure 16 illustrates good agreement between the measured (symbols) and SPICE-modeled (dashed lines) characteristics at 24 °C (black) and 500 °C (grey). Despite the large temperature difference, there is almost no difference in the low-frequency amplifier gain. Such behavior arises from the fact that the inv-amp drain resistor's value (R_{DD}) increases with temperature at about the same rate that the transistor's g_m decreases (i.e., the trends illustrated in Fig. 6). This reflects the fact that these parameters are oppositely linked to the conductivity of the 6H-SiC *n*-channel layer [6, 10, 13–15, 46, 48]. Thus, the $R_{DD} \times g_m$ product that governs the amplifier circuit's low-frequency voltage gain changes little with temperature.

While this basic approach to amplifier circuit temperature stability is not new (see [51, 52]), this work experimentally verifies its applicability to 6H-SiC JFET ICs operating over perhaps the widest temperature range ever demonstrated for a semiconductor transistor IC. It also points out a significant advantage of implementing on-chip resistors using the SiC n-channel that is common to the JFET n-channels, as opposed to implementing on-chip resistors via thin film resistive film depositions. Note, however, that the roughly 3-fold changes in R_{DD} and g_m (Fig. 6) do precipitate a corresponding drop in 500 °C corner frequency compared to 24 °C, as shown in Fig. 16. As confirmed by SPICE simulations, the amplifier's frequency performance is primarily limited by resistive-capacitive (RC) charging time of the output terminal whose capacitance is dominated by off-chip wiring and probe.

As described elsewhere [18, 20, 34, 35, 53], quite similar results were obtained from the NASA differential amplifier chip depicted in the abstract figure. The packaged single-chip amplifiers demonstrated extremely stable operation at 500 °C for thousands of hours (Section 3.4). Circuit design optimization (not undertaken in this initial NASA study) should enable much greater gain and bandwidth to be realized in single-chip amplifier ICs without sacrificing 500 °C operational durability. Likewise, implementation of these circuits in 4H-SiC polytype, which has about 2X higher electron mobility μ_n than 6H-SiC, should also enable better amplifier IC performance.

3.2 Digital logic integrated circuits Digital logic gate IC chips were implemented and packaged from the NASA-fabricated 6H-SiC JFET wafer. The basic approach for the logic implemented is illustrated by the Fig. 17 schematic of a digital inverter (i.e., NOT) gate.

This particular prototype family featured negative logic voltage levels and two power supplies (positive $+V_{DD}$ and

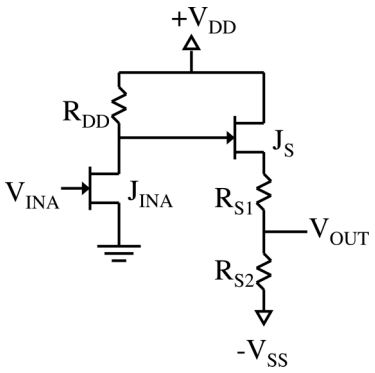


Figure 17 Schematic diagram of prototype NOT logic gate integrated circuit test chip implemented at NASA using n-channel depletion-mode 6H-SiC JFETs and resistors. The circuit operates with two power supplies ($+V_{DD}$ and $-V_{SS} = V_{Substrate}$) and negative logic signal voltages [54, 55].

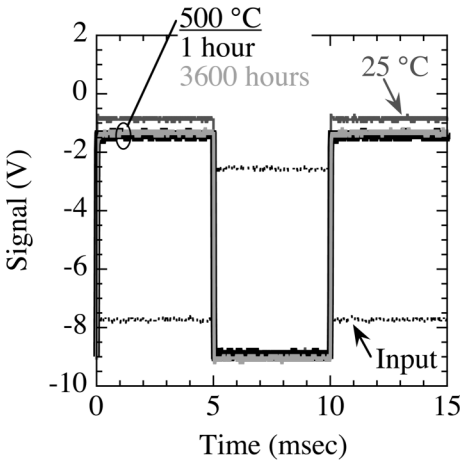


Figure 18 Experimentally measured NOT gate IC test waveforms showing that similar output is obtained at 25 °C and at the start (1 hour) and end (3600 hours) of prolonged 500 °C operational testing [20].

negative $-V_{SS}$ in the range of 18 V to 25 V). The negative logic levels ensure that input-stage (i.e., inverting amplifier stage) p^+ JFET gates are reverse-biased (with low leakage current) with respect to JFET n-channels. Given sufficient $I_{DSS} > V_{DD}/R_{DD}$ for JFET J_{INA}, the input logic voltage V_{IN} drives the inverting amplifier stage output (drain of JFET J_{INA} in Fig. 17) to near $+V_{DD}$ (for $V_{IN} = V_{IL}$ = logic low input voltage) or near ground (for $V_{IN} = V_{IH}$ = logic high input voltage). This feeds a level-shifter stage (JFET J_S and resistors R_{S1} and R_{S2}) that translates the inverting amplifier output V_{OUT} back to desired negative logic gate output voltages (V_{OH} or V_{OL}) that would successfully drive the input of a subsequent gate of this logic family. To avoid forward-biasing the channel-to-substrate n-to-p junction diode, the p-type substrate is biased at $V_{Substrate} = -V_{SS}$. This negative substrate bias slightly reduces the (negative) magnitude of JFET V_T and increases channel resistor values somewhat via substrate body bias effect [43–45]. It should be noted that the nominal implementation of this logic family, in which $R_{SS} = R_{S1} = R_{S2}$ and $|V_{SS}| = V_{DD}$ [54, 55], was not realized in the initial NASA experiments.

Figure 18 shows nearly temperature-independent output characteristics from a packaged NOT gate at 25 °C and 500 °C. The layout for this particular NOT gate was a 70 square R_{DD}, 13 square $R_{S1} = R_{S2}$, and 20µm/10 µm J_{INA} and J_S JFETs. The circuit was driven by the same power supply voltages of $V_{SS} = -20$ V and $V_{DD} = 24$ V at both temperatures. As with the other circuits described in this paper, the major effect of increasing temperature on the digital circuits was significantly decreased operating speed. With this NOT gate directly driving the wires leading out of the test oven to the oscilloscope probe, the measured signal propagation time increased from 1.7 µsec at 25 °C to about 6 µsec at 500 °C. This propagation time increase with temperature is on par with the increase in the resistivity of the n-type 6H-SiC channel. Even at 500 °C, greatly improved switching speed performance should be readily achievable via commonly employed digital integrated circuit design optimization, such as shorter transistor gate lengths, refined load (resistor or transistor), output buffering, etc. [43].

3.3 JFET IC durability at 500 °C Table 2 summarizes the long-term 500 °C oven-testing results from prototype packaged JFETs and ICs at NASA. The V_{max} column in Table 2 indicates the largest voltage difference applied to each chip throughout the 500 °C test ($V_{max} = V_{Dmax} + |V_{Gmax}|$ for discrete JFETs, $V_{max} = V_{DD} + |V_{SS}|$ for ICs). As demonstrated in Fig. 18, the packaged NOT gate successfully operated for over 3600 hours at 500 °C with only a slight change in output signal. Similar results were obtained for a 2-input NOR gate and a 2-input NAND gate that were also packaged and tested for thousands of hours at 500 °C [20, 34, 53, 56, 57]. These 2-input gates were implemented by adding a second input transistor in parallel (NOR) or series (NAND) to the first input transistor J_{INA} of

Table 2 Summary of long-term 500 °C 6H-SiC JFET IC operational testing results to date at the NASA Glenn Research Center.

packaged device	duration (hours)	V_{max} (V)	notes
100 µm/10 µm JFET	10,000	66	test ended – no failure
200 µm/10 µm JFET	10,000	66	test ended – no failure
40 µm/10 µm JFET #1	3380*	66	test still running
40 µm/10 µm JFET #2	2149*	66	test still running
40 µm/10 µm JFET #3	2149*	66	test still running
diff-amp IC	6519	40	sudden failure
inverting amp IC #1	3904	40	sudden failure
NOT gate IC	3600	44	sudden failure
NOR gate IC	2405	44	sudden failure
NAND gate IC	3380*	44	test still running
inverting amp IC #2	2455	20	sudden failure

* Includes over 190 thermal cycles between 24 °C and 500 °C.

Fig. 17. Due to circuit layout differences, the NOR gate required slightly different supply voltages ($V_{SS} = -24$ V and $V_{DD} = 20$ V) in order to operate near the same −2.5 V to −7.5 V logic levels as the NOT gate. For over 100 hours of the 500 °C operational test, the output of the NOT gate was wired directly to, and successfully drove, one of the NOR gate inputs. The NOR and NOT logic gates failed suddenly after 2400 and 3600 hours of respective 500 °C operational testing. Simple prototype amplifier stages achieved similar 500 °C operational durability.

The 500 °C stability of the packaged NASA JFET IC chips is illustrated by data presented in Fig. 19. Figure 19a plots normalized (to gain A_0 recorded 100 hours into the test) low-frequency amplifier voltage gains recorded throughout the course of 500 °C oven testing. The differential amplifier chip exhibited some changes in gain before the 2000 hour mark of 500 °C testing, after which its gain stabilized to within 3% of A_0 until sudden circuit failure occurred. The inverting amplifier's gain never varied by more than 3% prior to its sudden failure near 3900 hours of successful 500 °C operation. Figure 19b plots the change in output high (V_{OH}) and output low (V_{OL}) logic voltages recorded during the prolonged 500 °C NOT gate test. The logic gate ouputs changed by less than 200 mV until sudden circuit failure occurred at 3600 hours of 500 °C operation. The NASA test chips demonstrate a degree of stability and durability unprecedented for semiconductor integrated circuits operating in $T > 300$ °C ambient.

The fact that no discrete JFETs have failed while integrated circuits have failed over the similar 500 °C testing durations suggests that the observed circuit failures are due to degradation of the metal/dielectric interconnect stack. Figure 20 compares the optical appearance of (a) an as-fabricated chip, and (b) a packaged chip that was exposed

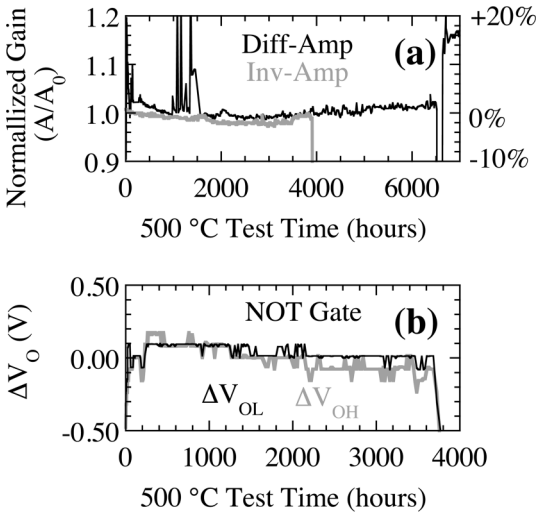


Figure 19 Normalized output signal history of NASA-fabricated 6H-SiC test ICs as a function of 500 °C operational test time. (a) Low frequency (1–2 kHz) gains of differential amplifier (black) and inverting amplifier (grey) chips. (b) Change in NOT gate output voltage for logic low (black) and logic high (grey).

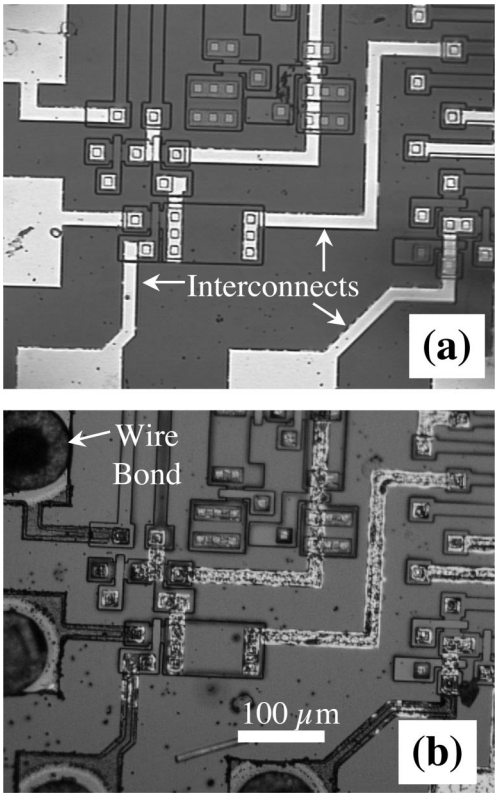


Figure 20 Optical micrographs of portions of NOT gate IC chips. (a) An as-fabricated chip prior to packaging. (b) A packaged chip following failure after thousands of hours operating at 500 °C [53].

to thousands of hours of 500 °C operation [53]. Significant physical changes occurred to the air-exposed interconnect metallization during the 500 °C test, especially in the vicinity of the gold wire bonds. Initial probe testing of metal traces across two failed chips has documented a few examples of separate interconnect traces demonstrating poor electrical isolation from each other. These near-short circuits indicate that loss of dielectric layer insulating property occurred in at least some localized regions. This probe testing has also revealed a few examples of near-open (poor conductance) interconnect traces. To date there has been no observed failure of packaging or gold wire bonds, and only one failure of an ohmic contact to an n-type SiC epitaxial resistor. Recently initiated materials analysis of failed chips should enable important insights into root chemical and physical mechanisms causing chip failures so that they may be reported and mitigated in future work.

4 Summary & future work

4.1 Process technology refinement For many envisioned applications, far greater circuit complexity than the few-transistor ICs demonstrated in this initial work will be needed. Reduction of device dimensions and operating biases, and implementation of multilayer interconnects are obvious important further steps towards realizing durable

500 °C SiC integrated circuitry with greater complexity, higher frequency performance, and increased functionality. Passivation of the topmost interconnect metal with dielectric is a silicon-industry standard processing step that could also improve the extreme temperature durability of future prototype SiC JFET ICs.

Processing related to reduction of the relatively large dimensions (10 μm) used in this initial work appears relatively straightforward. However, further miniaturization will correspondingly increase current densities and electric fields in the operating chip. As such changes have often led to durability/reliability challenges throughout the development history of silicon-based ICs, it naturally will be important to accumulate similar fundamental understanding of scaling and reliability tradeoffs as extreme temperature SiC ICs are further developed.

4.2 Circuit development Extreme temperature silicon carbide integrated circuits are in their infancy, somewhat analogous to silicon room-temperature ICs in the early 1960s before the silicon MOSFET became viable. In order to advance the state of the technology, much work remains to be done in modeling, amplifier design, logic circuits, all of which could enable complete microsystems operating at the extreme temperatures found in energy producing and consuming systems, such as found in aerospace propulsion. In regards to modeling, we have found that the 3/2-power model originally developed for silicon JFETs is very much applicable to the SiC JFETs, but high-speed/wide-bandwidth integrated circuits will require accurate capacitance modeling, which has not yet been addressed. Complex analog ICs would benefit from modeling of the fourth terminal, (i.e., the substrate back-gate effect) and this work has already been undertaken at CWRU [41]. In order to reach a wider community of designers, these models should be incorporated in the industry standard circuit simulator, SPICE, and this work has already begun both at CWRU and at NASA.

Researchers at CWRU have also begun to design advanced amplifiers, including fully differential, multi-stage amplifiers for interfacing to Wheatstone bridge sensors and monolithic transimpedance amplifiers for interfacing to capacitive or resonant microsensors that are commonly fabricated in MEMS technology [58]. In contrast to CMOS technology, silicon JFET technology is not readily amenable to switched-capacitor circuits, primarily due to their depletion-mode behavior and the difficulty of providing appropriate clock levels. It is interesting to note, however, that due to its wide bandgap voltage, it is possible to fabricate a SiC JFET that has a positive threshold voltage, as illustrated in Eq. (7). This would necessitate a pinch-off voltage less than 3 V, i.e., would require a tight process control over the active layer thickness and impurity concentration that is not within commercial SiC tolerances for commercial SiC epilayers [59]. A JFET having positive threshold voltage would also greatly simplify the design of logic circuits, although the lack of a complementary device will limit the SiC JFET logic circuits to rudimentary control functions.

Integrated amplifiers and control circuits could be monolithically integrated with SiC MEMS sensors and actuators to form microsystems that can operate in extreme environments. SiC MEMS sensors for pressure, acceleration, and strain have already been demonstrated, as have resonant structures that could serve as a time-base for local oscillators needed to excite sensors and for communications. In addition to sensors and actuators, integrated inductors and capacitors could be combined with the SiC integrated circuits to enable wireless powering and communications, which would greatly simplify the interconnection problems encountered in extreme environments.

4.3 Summary This work has experimentally demonstrated prototype semiconductor ICs with unprecedented stability and operational lifetime at 500 °C. Simple analog amplifier and digital logic gate chips fabricated using 6H-SiC JFET technology successfully operated in a laboratory oven for thousands of hours at 500 °C with little change in functional input/output characteristics. This result was achieved with chips (and their interconnect metallization) directly exposed to oxidizing air ambient in lidless high temperature packages. These prototype circuits also demonstrated nearly temperature-independent low-frequency functional characteristics (without changes to input signals or power supply voltages) across the very broad 25 °C to 500 °C temperature range. Such temperature-independent circuit behavior is enabled by the fact that each circuit's 6H-SiC resistors and transistors share a common n-channel structure with common temperature-dependent conducting properties. The primary impact of increasing ambient temperature on circuit operation was decrease of maximum operating frequency. This frequency decrease with temperature corresponds to increasing n-channel resistance well known to arise from reduced channel electron mobility via increased thermal phonon scattering. Advanced designs for higher-gain and higher bandwidth extreme temperature SiC JFET differential amplifier circuits have been demonstrated.

Although only a small number of devices have been packaged and tested for thousands of hours at high temperature, this demonstration establishes the initial feasibility of producing simple SiC integrated circuits that are capable of prolonged 500 °C operation. The increased 500 °C IC durability and stability experimentally demonstrated in this work is now sufficient for sensor signal conditioning circuits in jet-engine test programs. Nevertheless, substantial further testing and validation of this technology is needed prior to actual insertion into most applications. Long-term testing of additional packaged devices, including testing under more aggressive and realistic environmental conditions (including thermal cycling, thermal shock, vibration at high temperature, etc.), is planned. Likewise, future investigations of root failure mechanisms should provide valuable insights to help guide future chip

fabrication process refinements to enable realization of even better 500 °C IC durability.

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